

Module 3.0

Introduction to Switched Mode Power Supplies.

SMPS circuits are considerably more complex than the linear stabilised power supplies described in Power Supplies Module 2. The main advantage of this added complexity is that switched mode operation gives stabilised designs that can deliver more power for a given size, cost and weight of power unit.

A number of different design types or topologies are used. Where the input is the AC mains (line) supply the AC is rectified and smoothed by a reservoir capacitor before being processed by what is in effect a DC to DC converter, to produce a regulated DC output at the required level. Hence a SMPS can be used to convert AC to DC, such as in a desktop computer power supply, or DC to DC, either step up or step down in many different battery powered systems.

Fig. 3.0.1 shows a block diagram example of a typical SMPS with an AC Mains (line) input and a regulated DC output. The output rectification and filter are isolated from the High Frequency switching section by a high frequency transformer, and voltage control feedback is via an opto isolator. The control section is typical of specialist ICs containing HF oscillator, pulse width modulation, voltage and current control and output shut down sections.

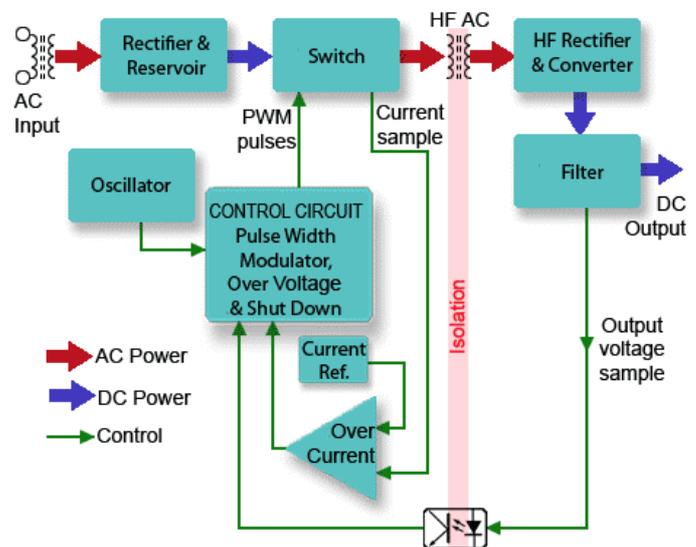


Fig.3.0.1 Typical SMPS Block Diagram

Whatever the purpose of a SMPS, a common feature (after conversion of AC to DC if required) is the use of a high frequency square wave to drive an electronic power switching circuit. This circuit switches the direction of the supply current in the primary winding of a transformer at typically 20kHz to 100kHz. A high frequency, high current AC is therefore produced in the transformer secondary. This may be rectified and smoothed in a number of ways to produce a stabilised DC supply of either a higher or lower level than the input voltage, depending on the topology used.

By using an oscillator and switch in this way to convert DC into AC, the switched mode technique can also be used as an 'inverter' to create an AC supply at mains potential from a DC battery supply.

In most switched mode supplies, regulation of both line (input voltage) and load (output voltage) is normally provided. This is achieved by altering the mark to space ratio of the oscillator waveform before applying it to the switches. Control of the mark to space ratio is achieved by comparing voltage feedback from the output of the supply with a stable reference voltage. Both over voltage and over current may also be provided.

Where it is important to maintain electrical isolation from the mains supply, this is provided by using a transformer, either at the AC input where it may also be used to alter the AC voltage prior to rectification, or between the control section of the power supply and the output section where, as well as providing isolation, a transformer with multiple secondary windings can produce several different voltage outputs.

To provide efficient regulation, a sample of the DC output voltage is normally fed back to the control circuitry and compared with a stable reference voltage. Any error produced is used to control the output voltage. To maintain electrical isolation between input and output, feedback will usually be via a device such as an opto-isolator.

Using high frequency for the switching drive gives several advantages:

- The transformer will be of a HF type, which is much smaller than a standard mains transformer.
- The ripple frequency will be much higher (e.g. 100kHz) than in a linear supply, and so it needs a smaller value of smoothing capacitor.
- Also using a square wave to drive the switching transistors (switched mode operation) ensures that they dissipate much less power than a conventional series regulator transistor. Again this means that smaller and cheaper transistors can be used, than in similarly rated linear power supplies.
- The use of smaller transformers and smoothing capacitors makes switched mode power supplies lighter and less bulky. The added cost of the complex control circuitry is also offset by the smaller, and therefore cheaper transformers and smoothing capacitors, making some switched mode designs less expensive than equivalent linear supplies.

Although linear supplies can provide better regulation and better ripple rejection at low power levels than switched mode supplies, the above advantages make the SMPS the most common choice for power supply units in any equipment where a stabilised supply is needed to deliver medium to large amounts of power.

A disadvantage of using such a high frequency square wave in a powerful circuit such as a SMPS is that many high power harmonics are created, so that without very effective RF screening and filtering, there is a danger of the SMPS creating RF interference.

Module 3.1

The Buck Converter

The Buck Converter uses the energy stored in the inductor L, during the on periods of the switching transistor output to supply the load during the off periods. The circuit operation depends on what is also sometimes called a Flywheel Circuit. This is because the circuit acts rather like a mechanical flywheel that, given regularly spaced pulses of energy keeps spinning smoothly (outputting energy) at a regular rate.

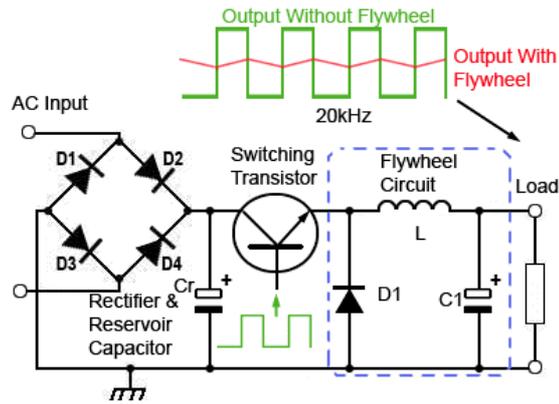


Fig. 3.1.1 The Buck Converter

The buck converter is a form of DC to DC converter, which can take a DC input directly from a DC source, such as a battery, or as shown in Fig. 3.1.1 from the rectifier/reservoir capacitor circuit. This DC is then converted to AC, using a switching or ‘chopper’ transistor, driven by a (usually pulse width modulated) high frequency square wave. This square wave is then re-converted to DC. Variations of this basic circuit can be used to take an AC input at high voltage directly from the mains (line) supply, or at a lower voltage via a step down transformer.

Buck Converter Operation

As shown in Fig. 3.1.1 the buck Converter circuit consists of the switching transistor, together with the flywheel circuit (D1, L1 and C1). While the transistor is on, current is flowing through the load via the inductor L1. The action of any inductor opposes changes in current flow and also acts as a store of energy. In this case the switching transistor output is prevented from increasing immediately to its peak value as the inductor stores energy taken from the increasing output; this stored energy is later released back into the circuit as a back e.m.f. as current from the switching transistor is rapidly switched off.

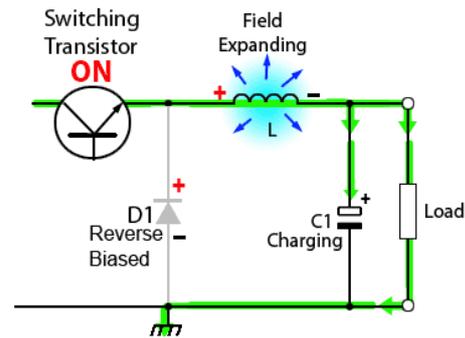


Fig. 3.1.2 Switching Transistor on

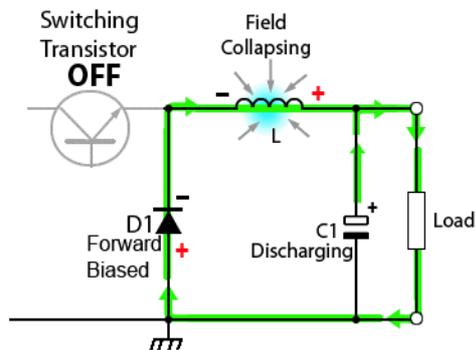


Fig. 3.1.3 Switching Transistor off

In Fig. 3.1.2 therefore, when the transistor Tr1, is switched on it is supplying the load with current. Initially current flow to the load is restricted as energy is also being stored in L1, therefore the current in the load and the charge on C1 builds up gradually during the ‘on’ period. Notice that throughout the on period, there will be a large positive voltage on D1 cathode and so the diode will be reverse biased and therefore play no part in the action.

When the transistor switches off as shown in Fig 3.1.3 the energy stored in the magnetic field around L1 is released back into the circuit. The polarity of the voltage across the inductor (the back e.m.f.) is in reverse to that during the ‘on’ period, and sufficient stored energy is available

in the collapsing magnetic field to keep current flowing at least part of the time the transistor switch is open.

The back e.m.f. from L1 now causes current to flow around the circuit via the load and D1, which is now forward biased. Once the inductor has returned a large part of its stored energy to the circuit and the load voltage begins to fall, the charge stored in C1 becomes a source of current, keeping current flowing through the load until the next 'on' period begins.

The overall effect of this is that, instead of a large square wave appearing across the load the ripple waveform is a small amplitude high frequency triangular wave with a DC level of:

$$V_{out} = V_{in} \times (\text{On time of switching waveform} / \text{periodic time of switching waveform})$$

$$\text{or: } V_{OUT} = V_{IN} \frac{t_{ON}}{T}$$

Therefore if the switching waveform has a mark to space ratio of 1:1 the output V_{OUT} from the buck Converter circuit will be half of V_{IN} . However if the mark to space ratio of the switching waveform is varied, any output voltage between approximately 0V and V_{IN} is possible.

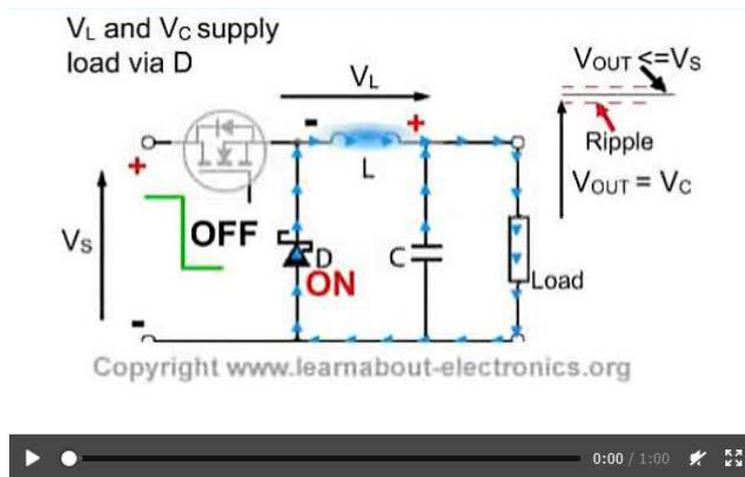


Fig. 3.1.4 Buck Converter Operation

Note: Fig 3.1.4 is an animated video only available in the on line version of this page.

Buck Converter for Negative Supplies

In many complex circuits, the main DC supply may be at a too high voltage for some parts of the circuit. E.g. a 24Vdc supply for an output stage may need to be reduced to 5V or 3.3V for logic circuits driving the output stage. In some circuit it may also be necessary to also cater for negative supplies. For such circumstances the circuit shown in Fig. 3.1.5 can be used. This involves a change around in the positions of L1 and D1, and reversing the polarity of C compared to the circuit in Fig 3.1.4. This variation of the basic buck converter now inverts the positive DC input to produce a negative supply in the range of 0V to $-V_{IN}$.

How Fig. 3.1.5 Works

When the transistor switch turns on the positive supply voltage is applied to L1. The diode D1 is reverse biased at this moment, so the supply current cannot reach the output, but charges L1, creating a magnetic field to build up around it. Notice that the voltage across L1 at this time causes the top of the inductor to be positive with respect to the 0V line.

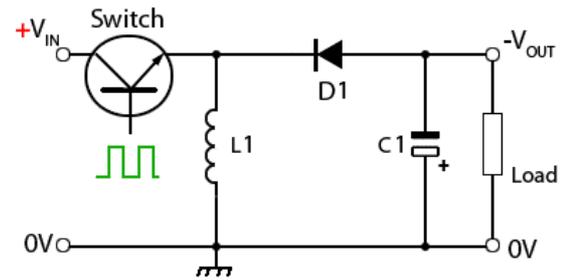


Fig. 3.1.5 Negative Buck Converter

When the input transistor switches off however, the magnetic field around L1 begins to collapse, and so induces a reversal of voltage across L1 that now makes the top of L1 negative with respect to 0V. At this time D1 becomes forward biased and conducts, causing the capacitor C1 to charge up producing a negative output voltage across the load. The actual value of negative output voltage will be the inverse of some fraction of the input voltage and depends on the mark to space ratio of the square wave signal applied input switch, which will be a pulse width modulated signal, typically operating at a constant frequency at tens of KHz.

Module 3.2

Boost Converter

Switched mode supplies can be used for many purposes including DC to DC converters. Often, although a DC supply, such as a battery may be available, its available voltage is not suitable for the system being supplied. For example, the motors used in driving electric automobiles require much higher voltages, in the region of 500V, than could be supplied a battery alone. Even if banks of batteries were used, the extra weight and space taken up would be too great to be practical. The answer to this problem is to use fewer batteries and to boost the available DC voltage to the required level by using a boost converter. The voltage output of all batteries, large or small, varies as the available charge is used up, but the useful amount of charge in a battery can be extended if the dwindling voltage can be boosted back up to a useful level, again by using a boost converter.

The DC input to a boost converter can be from many sources as well as batteries, such as rectified AC from the mains supply, or DC from solar panels, fuel cells, dynamos and DC generators. The boost converter is different to the Buck Regulator in that it's output voltage is greater than its input voltage. However it is important to remember that, as power ($P = \text{voltage (V)} \times \text{current (I)}$), if the output voltage is increased, then provided no extra power is created in the system, the output current must decrease.

As Fig. 3.2.1 illustrates the basic circuit of a Boost converter. However, in this circuit the switching transistor is a power MOSFET. The rest of the components are the same as those used in the buck converter illustrated in Fig. 3.1.2, except that their positions have been rearranged.

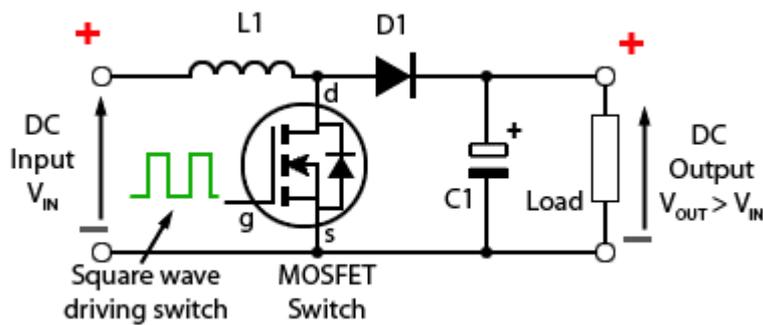


Fig. 3.2.1 Basic Boost converter Circuit

Boost converter Operation

The switching MOSFET has a high frequency square wave applied to its gate terminal. During the high period of the wave, the MOSFET is turned on, placing a short circuit from the right hand side of L1 to the negative input supply terminal. Therefore a current flows between the positive and negative supply terminals through L1, which stores energy in its magnetic field. There is virtually no current flowing in the remainder of the circuit as

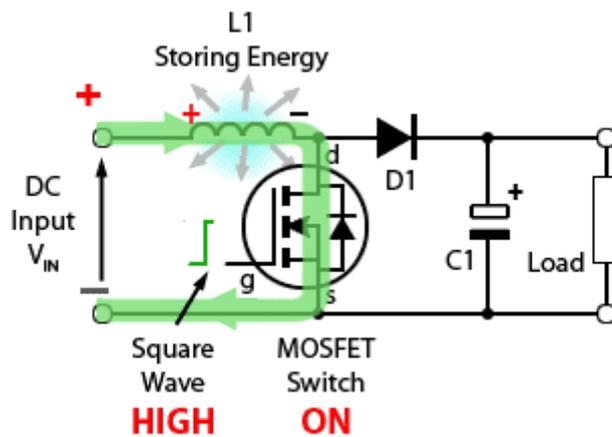


Fig. 3.2.2a Boost Converter Operation at Switch On

D1, C1 and the load represent a much higher impedance than the path directly through the conducting MOSFET. (See Fig. 3.2.2a).

In the low part of the square wave cycle, the MOSFET is rapidly turned off. L1 opposes the sudden reduction in current by producing a back e.m.f. in the opposite polarity to the voltage across it during the ON period, to keep current flowing. As can be seen from Fig. 3.2.2b this results in two voltages, the supply voltage and the back e.m.f. of L1 in series with each other, which add to produce a higher voltage ($V_{IN} + V_L$).

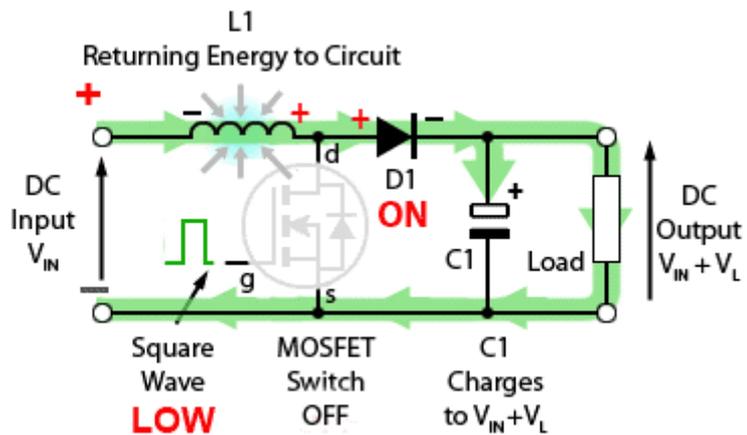


Fig. 3.2.3b Current Path With MOSFET Off

This voltage (now that there is no current path through the MOSFET) forward biases D1 and charges up C1 to $V_{IN} + V_L$ minus the small forward voltage drop across D1, and also supplies the load.

Each time the MOSFET conducts, the voltage ($V_{IN} + V_L$) on the cathode of D1 due to the charge on C1, is more positive the voltage on D1 anode (0V due to the heavily conducting MOSFET). D1 is therefore turned off so the output of the circuit is isolated from the input, however the load continues to be supplied with $V_{IN} + V_L$ from the charge on C1, as shown in Fig.3.2.2c.

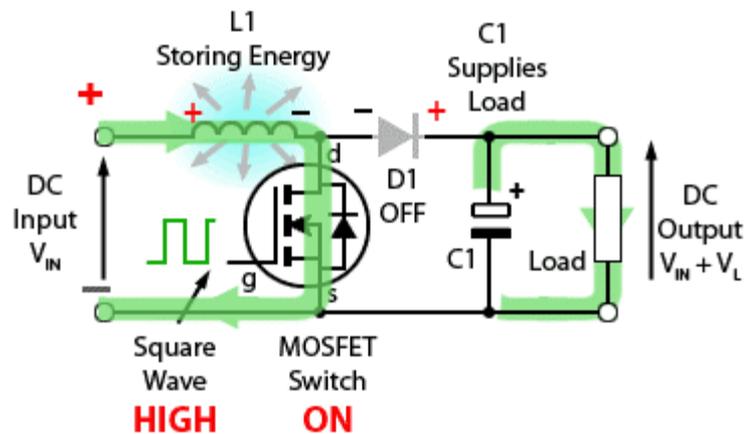


Fig. 3.2.3c Current Path With MOSFET On

The theoretical output voltage is determined by the input voltage divided by 1 minus the duty cycle (D) of the switching waveform, which will be some figure between 0 and 1 (corresponding to 0 to 100%) and therefore can be determined using the following formula:

$$V_{OUT} = \frac{V_{IN}}{(1 - D)}$$

Example:

If the switching square wave has a period of 10uS, the input voltage is 9V and the ON is half of the periodic time, i.e. 5uS, then the output voltage will be:

$$V_{OUT} = 9 / (1 - 0.5) = 9 / 0.5 = 18V \text{ (minus output diode voltage drop)}$$

Because the output voltage is dependent on the duty cycle it is important that the duty cycle is accurately controlled. For example if the duty cycle increase from 0.5 to 0.99 the output voltage produced would be:

$$V_{OUT} = 9/(1 - 0.99) = 9/0.99 = 900V$$

Before this level of output voltage was reached, however there would of course be some serious damage (and smoke) caused, so in practice the changes in duty cycle are kept much less than indicated in this example.

I.C. Boost Converter

Because of the ease with which boost converters can supply large over voltages, they will almost always include some stabilisation to control the output voltage. This will usually involve comparing a sample of the output voltage with a steady voltage reference, as described in series stabilised supplies. However in switched mode circuits, including boost converters, the resulting error voltage does not directly control the switching transistor, but is used to vary the duty cycle of the drive oscillator. A typical example of such an arrangement used in an I.C. boost converter is shown in Fig. 3.2.3.

This involves feeding back a portion of the output voltage to a control system as illustrated in Fig. 3.2.3, which shows a typical boost converter I.C., in this case the LM27313 from Texas Instruments. This chip is designed for use in low power systems such as PDAs, cameras, mobile phones, and GPS devices.

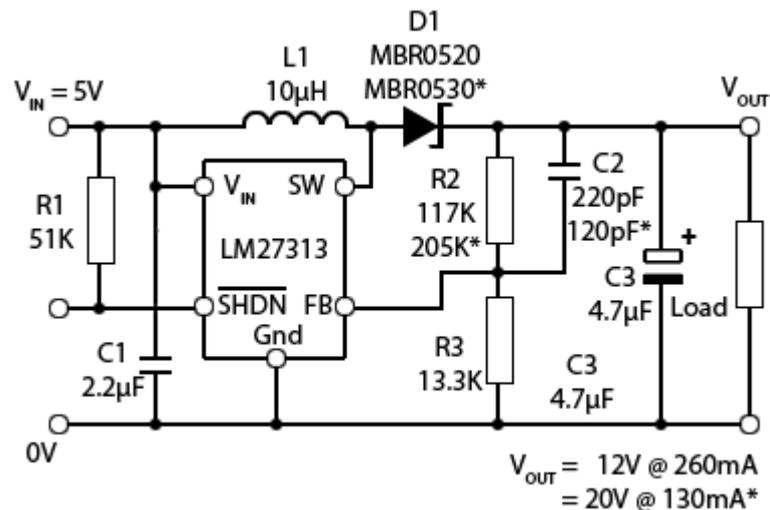


Fig. 3.2.3 Typical I.C. Boost Converter (LM27313)

The internal oscillator and FET switch switches the current through L1 at a fixed frequency of about 1.6Mhz. The I.C. also has a shut down (SHDN) facility, operated by external logic, by which the boost converter may be disabled when not required, to save battery power.

Protection Circuits

The feedback resistors R2 and R3 are used to feed back an appropriate fraction of V_{OUT} to the feedback pin of the I.C. The ratio of R2:R3 produces a sample proportional to the output voltage, which is used to alter the duty cycle of the switching oscillator waveform, enabling a range of automatically regulated boost voltages to be obtained. Other safety features provided by the I.C. are over current shut down, which disables the switch on a cycle-by-cycle basis if too much current is sensed. And an over temperature shut down facility. Notice also that a Schottky diode with an appropriate voltage and current rating is used for D1 to keep losses due to the forward voltage drop of the diode as small as possible.

Stability

Another problem facing designers of high frequency boost converters is that of stability, as at MHz frequencies both negative and positive feedback can occur simply due to electromagnetic fields radiating between components within the circuit, especially where the circuit components are in very close proximity as in surface mount layouts. C1 and C2 are therefore added to improve stability and reduce any HF being transmitted via the DC input. It would also be usual to feed the output of the converter via an additional LC low pass filter to remove any remaining ripple from the DC output.

Module 3.3

Buck-Boost Converters

A Buck-Boost converter is a switched mode power supply topology, which combines the principles of the Buck Converter and the Boost converter in a single circuit. Like other SMPS designs, it provides a regulated DC output voltage from either an AC or a DC input.

The Buck converter described in Power Supplies Module 3.1 produces a DC output in a range from 0V to just less than the input voltage. The boost converter will produce an output voltage ranging from the same voltage as the input, to a level much higher than the input.

There are many applications however, such as battery-powered systems, where the input voltage can vary widely, starting at full charge and gradually decreasing as the battery charge is used up. At full charge, where the battery voltage may be higher than actually needed by the circuit being powered, a buck regulator would be ideal to keep the supply voltage steady. However as the charge diminishes the input voltage falls below the level required by the circuit, and either the battery must be discarded or re-charged; at this point the ideal alternative would be the boost regulator described in Power Supplies Module 3.2.

By combining these two regulator topologies it is possible to have a regulator circuit that can cope with a wide range of input voltages both higher or lower than that needed by the circuit. Fortunately both buck and boost converters use very similar components; they just need to be rearranged, depending on the level of the input voltage. In Fig. 3.3.1 the common components of the buck and boost circuits are combined. A control unit is added, which senses the level of input voltage, then selects the appropriate circuit action. (Note that in the examples in this section the transistors are shown as MOSFETs, commonly used in higher power converters as they have a very low drain/source voltage when saturated, and the diodes shown as Schottky types, which also have a low forward junction voltage and are able to switch at high speeds).

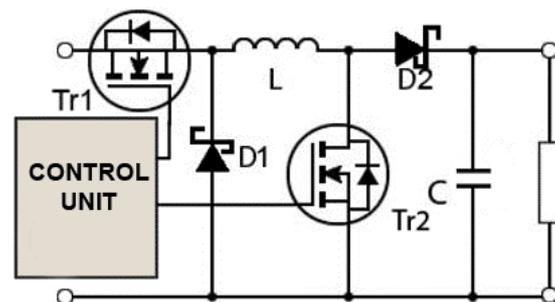


Fig. 3.3.1 The Buck and Boost Converters Combined

Operation as a Buck Converter

The basic operation of the buck boost converter are illustrated in Figs. 3.3.2 to 3.3.5

Fig. 3.3.2 shows the Buck converter action. Tr2 is turned off throughout the buck converter operation and Tr1 is turned on and off by a high frequency square wave from the control unit. When the gate of Tr1 is high current flows through L, charging its magnetic field, charging C and supplying the load. The Schottky diode D1 is turned off due to the positive voltage on its cathode.

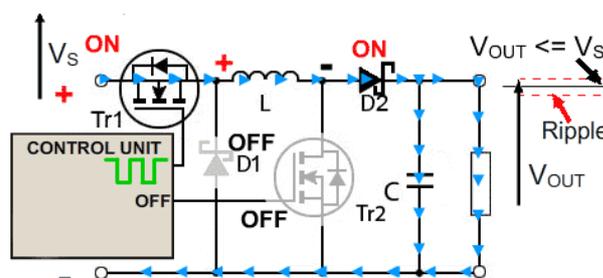


Fig 3.3.2 Buck Converter Action (1)

Fig 3.3.3 shows the current flow during the buck operation of the circuit when the control unit switches Tr1 off. The initial source of current is now the inductor L. Its magnetic field is collapsing, the back e.m.f. generated by the collapsing field reverses the polarity of the voltage across L, which turns on D1 and current flows through D2 and the load.

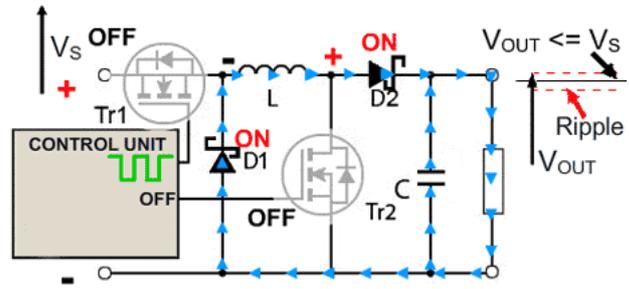


Fig 3.3.3 Buck Converter Action (2)

As the current due to the discharge of L decreases, the charge accumulated in C during the on period of Tr1 now also adds to the current flowing through the load, keeping V_{OUT} reasonably constant during the off period. This helps keep the ripple amplitude to a minimum and V_{OUT} close to the value of V_S .

Operation as a Boost Converter

In Boost Converter mode, Tr1 is on continually and the high frequency square wave applied to gate. During the on periods when conducting, the input current flows the inductor L and via Tr2, directly the supply negative terminal up the magnetic field around L. this is happening D2 cannot conduct anode is being held at ground by the heavily conducting Tr2. For duration of the on period, the load is being supplied entirely by the charge on the capacitor C, built up on previous oscillator cycles. The gradual discharge of C during the on period (and its subsequent recharging) accounts for the amount of high frequency ripple on the output voltage, which is at a potential of approximately $V_S + V_L$.

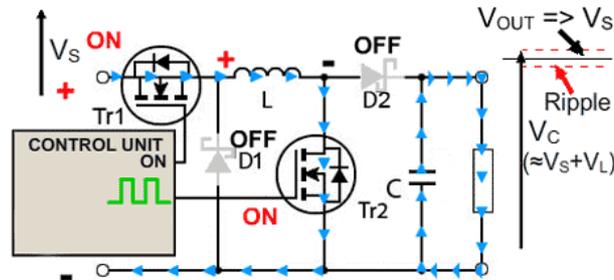


Fig 3.3.4 Boost Converter Action (1)

turned
Tr2
Tr2 is
through
back to
charging
Whilst
as its
potential
the

The Off Period

At the start of the off period of Tr2 L is charged and C is partially discharged. The inductor L now generates a back e.m.f. and its value depends on the rate of change of as Tr2 switches off and on the of inductance the coil possesses; therefore the back e.m.f can any over a wide range, depending on the of the circuit. Notice particularly that the polarity of the voltage across L has now reversed and so adds to the input voltage V_S giving an output voltage that at least equal to or greater than the input voltage D2 is now forward biased and so the circuit current supplies the load current, and at the same time re-charges the capacitor to $V_S + V_L$ ready for the next on period of Tr2.

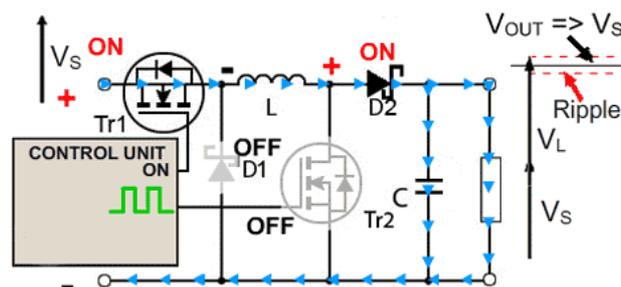


Fig 3.3.4 Boost Converter Action (2)

is
that
current
amount
voltage
design

There are a number of variations of this basic Buck Boost circuit, some designs working at lower frequencies may use bipolar transistors that have lower losses in their saturated state than MOSFETs, and the higher speed switching of MOSFETs is less of an advantage. In high

voltage designs, silicon diodes may be used in preference to Schottky types due to the silicon diode's higher reverse voltage capabilities. Another variation is to use synchronous switching where, instead of using diodes that simply respond to the voltage polarity across them, four synchronised (by the control unit) MOSFETs do all the switching.

The control unit will also carry out the normal pulse width modulation to regulate the output voltage as well as supplying over current and over voltage protection.

Another commonly used facility is 'pulse skipping' where the control unit prevents charging on one or more oscillator pulses when it senses that the load current is low. This reduces the overall current drawn from the (typically battery) supply, prolonging battery life.

Buck-boost Converter I.Cs. are also available to carry out the control unit functions. These range from very low power, high efficiency I.Cs. for portable devices such as mobile phones and automotive applications, such as the TPS63000 series from Texas Instruments, and the LTC3789 from Linear Technology, to large industrial high power DC-DC converters providing many kilowatts of output power.

Module 3.4

Push Pull Switched Mode Power Supply

Fig. 3.4.1 shows a block diagram of a switched mode power supply designed around a UC3524N Advanced Regulating Pulse Width Modulator by Texas Instruments.

The circuit is a DC to DC converter using a DC input of 15V to 30V and produces regulated 5V output at a up to about 250mA. The uses push pull power switching driving a high frequency transformer, which isolates the output circuit the input. The output is short protected, and the maximum manually set using adjustable limiting.

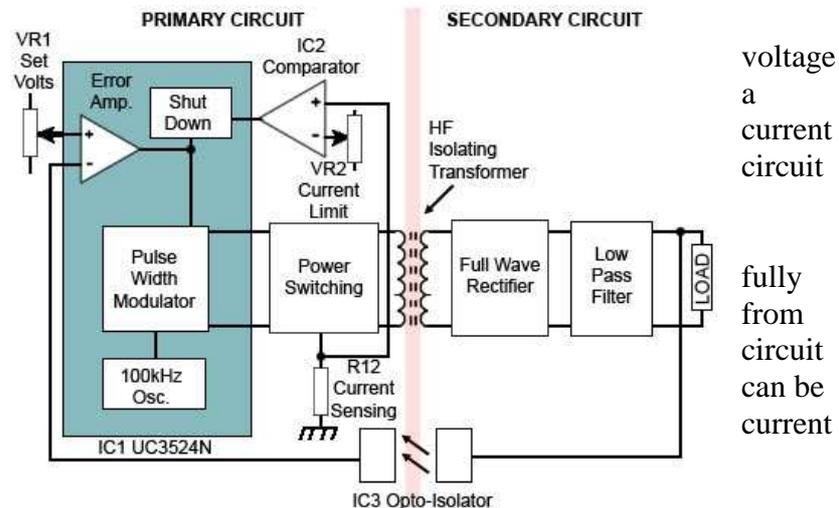


Fig. 3.4.1 Push Pull SMPS Block Diagram

Primary Circuit.

A 100kHz oscillator within IC1 (UC3524N) generates pulses, which are fed to the power switching transistors via a pulse width modulator (within IC1). The width of the drive pulses at the PWM output controls the length of time, for which the power switching transistors conduct, and therefore the amount of power delivered to the transformer.

The pulse width and therefore the output voltage is controlled by the error amplifier, which measures the difference between the voltage feedback via the opto-isolator, and a reference voltage set by Vr1) appearing at the output of the error amplifier within IC1. When the circuit output voltage is correct, these two voltages will be equal.

Over current protection is provided to ensure that the supply is shut down in the event of too high a current demand at the output. The output terminals can even be shorted together without damaging the supply.

Each pulse of current in the power switching transistors produces a voltage pulse across the sensing resistor R12. The amplitude of these pulses is proportional to the current being delivered to the transformer by the switching circuit. If the peak value of any of these pulses exceeds the DC voltage set by Vr2 (Current limit) then the output from IC2 will cause pulse width modulator input to reduce the width of the pulse being produced by the modulator at that time, momentarily reducing the output voltage. If the over current condition disappears, the output voltage will be restored to its normal level, but if the load current remains high, the current limiter will continue to reduce the pulse width, dependent on the amount of over current, even down to zero in the case of a short circuit output.

The Secondary Circuit

The push pull switching transistors create an AC waveform across the transformer primary winding and the secondary feeds a conventional full wave rectifier and LC low pass filter to

supply the load with a stable 5V at the output terminals. Negative feedback to the voltage stabilising circuit in the primary side of the circuit is via the opto-isolator (IC3). The higher the output voltage, the brighter the glow from an LED sealed within the secondary side, and the larger the output voltage derived from an opto-transistor in the primary side of the device.

Circuit Description

The full schematic diagram for the circuit is shown in Fig. 3.4.2.

The oscillator within IC1 produces narrow 100kHz (approx) pulses that are used as clock pulses for the Switch Logic within IC1; these can be monitored on pin 3. The timing components for the oscillator are R3 and C2. The charging ramp produced by C2 is also used as an input to the inverting input of the comparator.

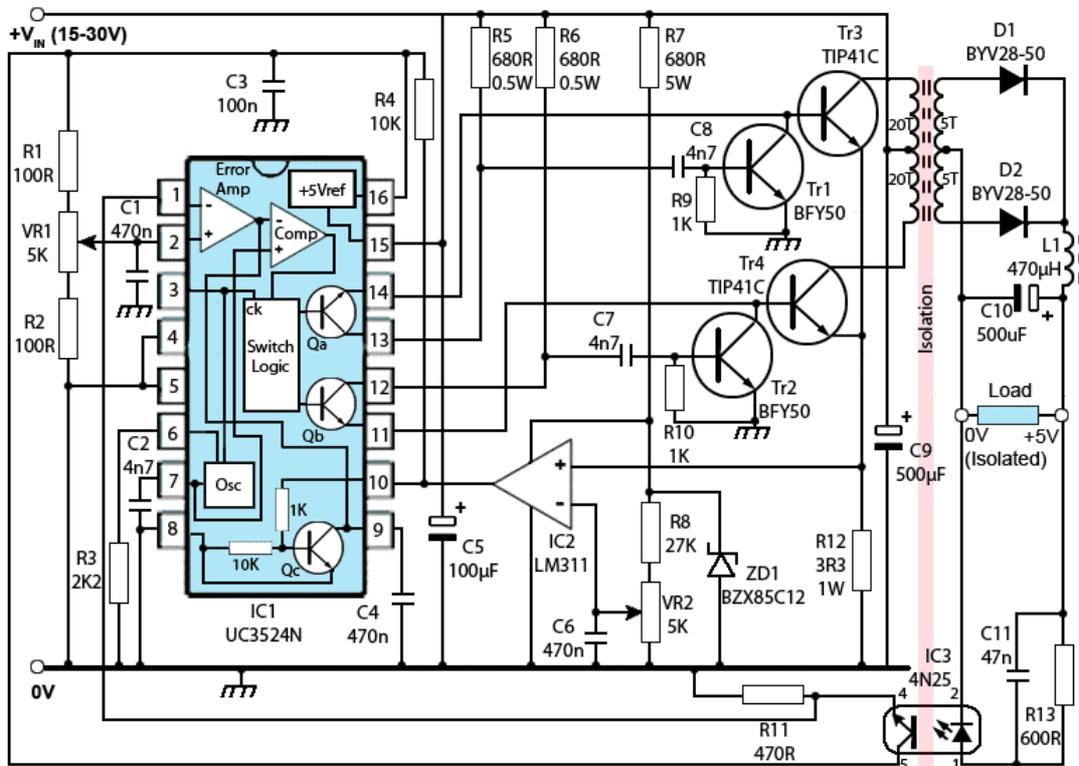


Fig. 3.4.2 Push Pull Switched Mode Power Supply

The pulse width modulator in IC1 comprises the comparator and the switching logic. The outputs of this block supply variable width pulses to the two transistors Qa and Qb. The error amplifier (with inputs from pins 1 and 2) compares the stable reference voltage (set by Vr1 supplied from an internally regulated 5V from pin 16) with a sample of the load voltage developed across the opto-isolator emitter resistor, R11. The resulting error voltage is used as the non-inverting input to the PWM comparator.

The facilities within the UC5324N used in this circuit are shown in more detail in Fig. 3.4.3 (Note: Some unused details of the UC3542N have been omitted for clarity, for more information see the Texas Instruments UC3542N data sheet).

Pulse Width Modulator

The action of the pulse width modulator, is described by the waveforms shown in Fig. 3.4 4 is as follows:

Clock pulses (CK) from the oscillator are fed to the Bi-stable (flip-flop) which produces a square wave with a 1:1 mark/space ratio and a frequency of 50kHz, (half that of the oscillator) at its Q output, and an inverted version of this wave at its output.

Each of these square waves, Q and \bar{Q} (the opposite of Q) provides an input to each of the NOR gates. The logic rules for a NOR gate are that its output will be high, only when all its three inputs are low. Notice that the Q and \bar{Q} signals go low on alternate clock pulse low states. The clock signal also provides an input to both NOR gates.

The third input to each of the NOR gates is provided by the comparator output, which is a series of variable width produced by comparing the DC error voltage from the error amplifier in IC1 with the ramp produced by the oscillator timing capacitor C4.

As each NOR gate output goes high, alternate pulses are produced at Qa and Qb bases whose width depends on the value of the error voltage, the lower the value of the error voltage (due to a higher value of "sample" voltage at pin 1) the narrower the pulses produced. These narrower pulses will in turn lead to a reduction in power in the transformer and a reduction in load voltage.

Power Switching Circuits

The internal drive transistors Qa and Qb each produce a pair of anti-phase pulses at their collector and emitter respectively. The emitter

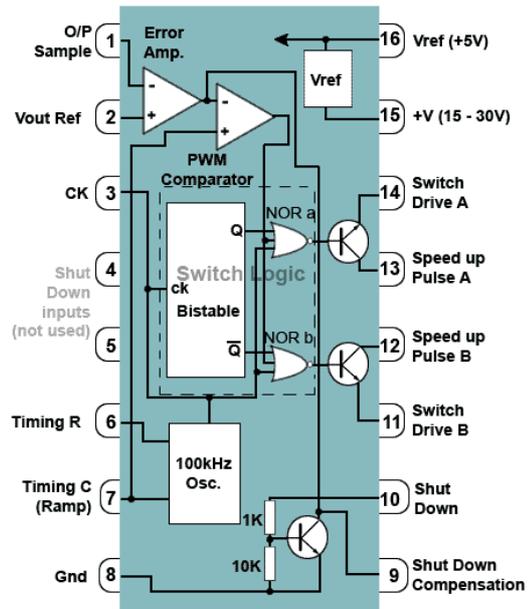


Fig.3.4.3 The UC3524N (part detail)

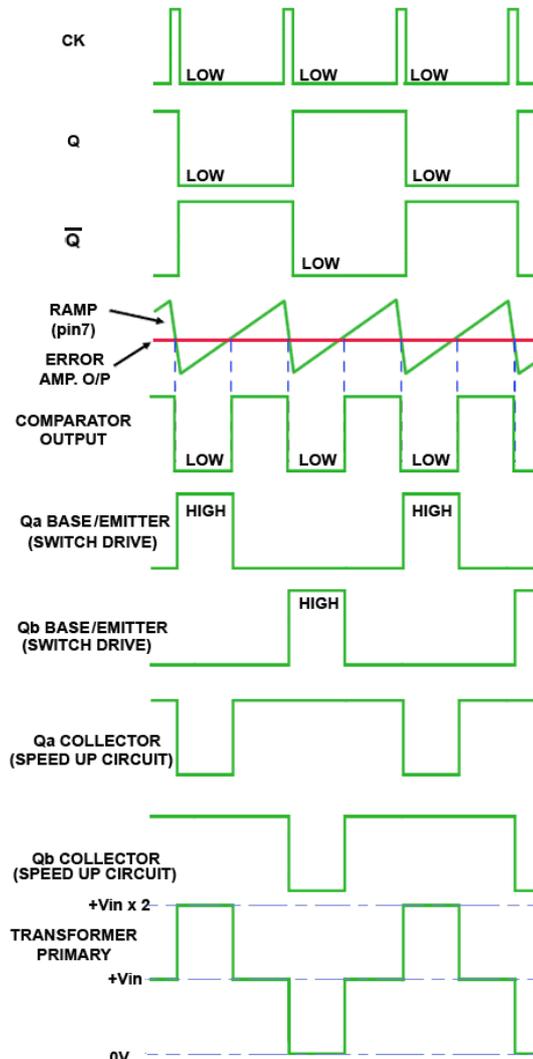


Fig. 3.4.4 UC3524N

signals driving the power switching transistors Tr3 and Tr4, and the collectors driving the speed up circuits Tr1/Tr2.

The reason for including the speed up circuits is to overcome the delay that would normally happen while the power switching transistors Tr3 and Tr4 are conducting, their base/emitter (which naturally forms a small capacitance) is charged up, and discharged before the transistor fully turn off.

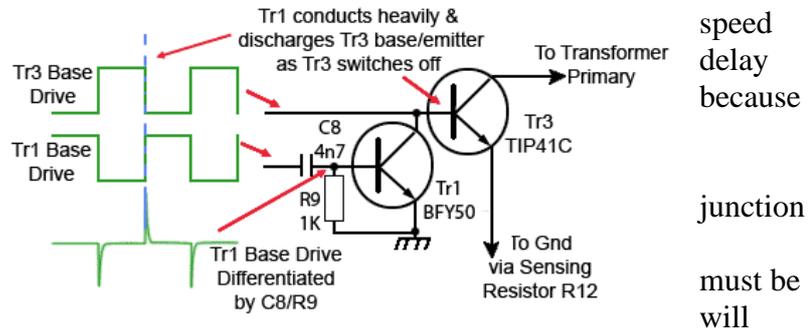


Fig. 3.4.5 Speeding up the Power Switch Turn Off

The power transistor junctions are rapidly discharged by momentarily turning on Tr1 or Tr2 using a differentiated pulse generated from the rising edge of the waveform from the collector of Qa or Qb in IC1, which of course happens at exactly the same instant as Tr3 or Tr4 is turning off, as illustrated in Fig 3.4.5.

Because the transformer primary centre tap is connected to the main (+V_{IN}) supply, it will always be at the supply potential. The collector voltages of Tr3 and Tr4 will also be at +V_{IN} during the periods when both transistors are turned off. During the 'on' pulse of Tr3 its collector will be at approximately 0V, and due to the centre tapping the bottom half of the primary will be in anti-phase to the top half so the collector of Tr4 will be positive at twice the value of +V_{IN} for the period of the Tr3 'on' pulse. This situation is reversed during the 'on' pulse of Tr4. This action produces a stepped type of waveform with amplitude of +V_{IN} x 2 across the primary winding as shown in Fig 3.4.4.

Because of the push pull topology used by this circuit, it is a simple matter to arrange for the circuit to have multiple outputs, of different (higher or lower) voltages by using a transformer similar to the one illustrated in Fig. 3.4.6, which has multiple secondary windings with appropriate turns ratios, provided the overall maximum current is not exceeded. Feedback however, would be taken from only one of the outputs to control all the voltage outputs.

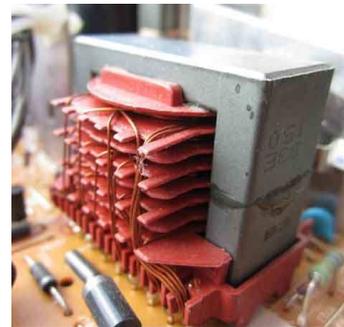


Fig. 3.4.6 Multi Secondary Transformer

The Secondary Circuit

The resulting secondary voltage is rectified by D1 and D2, smoothed by the low pass filter L1/C10 before being supplied to the load. The load voltage is sampled and fed to the LED within opto-isolator IC3 via the current limiting resistor R13.

Current limiting

Current limiting, which is capable of completely shutting down the circuit under extreme overload conditions is provided by the action of IC2 and the shut down transistor between pins 9 and 10 within IC1.

Pin 3 of IC2 is provided with a stable reference voltage derived from the shunt voltage regulator R7/ZD1 via the current limit control Vr2. The non-inverting input of IC2 is connected to a low value current sensing resistor R12 in the emitter lead common to both switching transistors Tr3/Tr4.

Every time either transistor conducts, the resulting emitter large current produced a voltage pulse across R12. The peak voltage of this pulse will be proportional to the emitter current flowing and therefore, also to the output current.

If the peak voltage of any pulse exceeds the stabilised voltage non-inverting input of IC2 a positive pulse will be produced at the output and the base of Qc within IC1. This will cause the collector voltage of this transistor to fall, so reducing the error voltage that is controlling pulse width in the pulse width modulator. This action has the effect of reducing the width of the pulse presently being produced, thus instantly reducing output voltage. If the current overload disappears, the pulse width modulator will return to normal operation. If not, subsequent pulses will be further reduced until the output voltage falls (if necessary) to zero.

In fact the action of the current limit circuit is not as instant as the above description suggests, due to the presence of C4 on the shut down compensation pin (9) of IC1. This capacitor tends to integrate the voltage changes on the collector of the shut down transistor so that rapid variations of the output voltage during current limiter action are avoided.